Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A sense amplifier for reading a memory cell, comprising:

a read node electrically coupled to the memory cell;

a first active branch connected to the read node and comprising means for supplying a read current at the read node; ~~and~~

a data output linked to one node of the first active branch at which a voltage representative of ~~the~~ a conductivity state of the memory cell appears~~,~~; and

a second active branch connected to the read node, comprising means for supplying, at the read node, a current that is added to the current supplied by the first active branch, such that the voltage representative of the conductivity state of the memory cell remains substantially stable upon a current draw at the read node.

2. (Original) The sense amplifier according to claim 1 wherein the first active branch is off and does not supply any current during the reading of an off or barely conductive memory cell.

3. (Original) The sense amplifier according to claim 1 wherein the first active branch comprises a first current generator linked to the read node, and the second read branch comprises a second current generator linked to the read node.

4. (Original) The sense amplifier according to claim 3 wherein the current generators comprise PMOS transistors driven by a common reference voltage.

5. (Original) The sense amplifier according to claim 3 wherein the second current generator supplies a current higher than a current supplied by the first current generator.

6. (Original) The sense amplifier according to claim 3 wherein the first current generator is linked to the read node through at least a first cascode transistor, and the second current generator is linked to the read node through at least a second cascode transistor.

7. (Original) The sense amplifier according to claim 3 wherein the first current generator is linked to the read node through at least a first MOS transistor, while the second current generator is linked directly to the read node, the read node being connected to a voltage-limiting diode.

8. (Original) The sense amplifier according to claim 1, further comprising:

a stage for controlling the first and the second active branches.

9. (Original) The sense amplifier according to claim 8 wherein the control stage controls the active branches such that a voltage appearing at the read node is regulated in the vicinity of a predetermined value.

10. (Original) The sense amplifier according to claim 8 wherein the control stage controls the active branches such that the first active branch does not supply current while the current supplied by the second active branch does not supply the maximum value of the current it can deliver.

11. (Original) The sense amplifier according to claim 8 wherein:

the control stage supplies a first gate control voltage to a first cascode transistor of the first active branch, and a second gate control voltage to a second cascode transistor of the second active branch, and

the first and second control voltages are controlled by the control stage such that the gate source voltage of the second transistor is higher than the gate source voltage of the first transistor.

12. (Original) The sense amplifier according to claim 11 wherein:
the first and second cascode transistors are N-type MOS transistors; and
the second control voltage is higher than the first control voltage.

13. (Original) The sense amplifier according to claim 11 wherein:
the control stage comprises a current generator in series with a load;
the first control voltage is taken off at the cathode of the load; and
the second control voltage is taken off at the anode of the load.

14. (Original) The sense amplifier according to claim 13 wherein the load is a resistance.

15. (Original) The sense amplifier according to claim 13 wherein the load is a MOS transistor.

16. (Original) The sense amplifier according to claim 1, further comprising a precharge transistor for supplying, during a precharge phase, a precharge current higher than the sum of the currents supplied by the first and the second active branches.

17. (Original) A non-volatile memory comprising a memory array comprising at least one memory cell, characterized in that it further comprises at least one sense amplifier according to claim 1 for reading the memory cell.

18. (Currently Amended) A sense amplifier for reading a memory cell, comprising:

a read node that is electrically connectable to a first terminal of a memory cell;

a first branch coupled to the read node, the first branch providing a first read current to the read node;

a second branch coupled to the read node, the second active branch providing a second ~~read~~ current to the read node;

a data sense node coupled to the first branch;

a voltage pick-up node within the first branch; and

a sense output node coupled to the voltage pick-up node within the first branch.

19. (New) The sense amplifier of claim 18 wherein the first and second currents are added such that a voltage at the data sense node representative of a conductivity state of the memory cell remains substantially stable upon current draw at the read node.

20. (New) The sense amplifier of claim 18, further comprising a pair of transistors at each of the first and second branches to respectively provide the first and second currents.